A Differential CMOS Automatic Gain Control Amplifier

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Abstract – In this paper, a differential CMOS automatic gain control amplifier is presented. The proposed architecture uses a differential variable gain amplifier, implemented with a Gilbert cell and provides an automatic gain control amplifier for both alternations of the input signal. It yields almost 20 dB dynamic range of input 100 MHz sinusoidal signal and provides a constant differential output of 200 mV pp with AGC loop bandwidth of 1MHz. The power consumption is 50 mW from a single 3.3 V voltage supply.

I. INTRODUCTION

The automatic gain control (AGC) amplifier and limiting amplifier are the two post-amplifier techniques for maintaining constant output signal amplitude against the input signal variation.

The different types of AGC are presented in literature [1] – [4].

We introduce in this paper a compact differential CMOS automatic gain control amplifier which can be found in numerous applications in communications systems and audio/video analog signal-processing circuits.

The block diagram of the proposed circuit is presented in Fig. 1. It is composed of a forward path and a feedback path. In the forward path, the variable gain amplifier (VGA) is controlled by a feedback low frequency path and the output differential currents given by VGA are transformed into voltages using a differential current to voltage converter. The AGC feedback path circuits shown in Fig. 1 include two peak detectors (for both alternations of the input signal) and an inverter summing amplifier.

The envelopes of the two alternations of the input signal are added and inverted and the resulted low frequency voltage signal is used in the feedback loop to control the VGA. Thus a signal with a constant magnitude is provided by the VGA implemented with a differential Gilbert cell. The proposed VGA provides two differential output currents with constant magnitude. For an optimal operating of the voltage mode peak detectors, the two differential currents provided by the VGA are converted into two differential voltages having a constant dc level of 1.5V.

The method’s principle of the proposed AGC architecture has been confirmed by system level simulations.

II. CIRCUIT DESCRIPTION

A. Variable Gain Amplifier

VGA is an amplifier stage whose gain can be adjusted using the information provided by the feedback loop. There are three basic types of VGA’s that are applicable in AGC: linear, exponential, and polynomial [1]. The exponential type is widely used because of its wider dynamic range [1].

In our design a VGA implemented by a differential Gilbert cell is used.

In Fig. 2, the electric scheme of the proposed variable gain amplifier is shown.

The main function of the peak detector is to extract the information about the amplitude of the forward path signal.
The operating of the proposed VGA is described in following.

First, the situation when resistor \( R_0 \) is not present (\( R_0 = 0 \)) in the electric scheme shown in Fig. 2 is analyzed. In this case a single bias current, having the \( I_{bias} \) value, is used.

The currents through transistors \( M_1 \) and \( M_2 \) can be written:

\[
\begin{align*}
I_1 &= I_{bias} + \frac{1}{4} \frac{\mu C_m}{W/L} V_{in1}^2 \cdot \frac{4I_{bias}}{\mu C_m \left( \frac{W}{L} \right)^2} - \frac{4I_{bias}}{\mu C_m \left( \frac{W}{L} \right)^2} \\
I_2 &= I_{bias} - \frac{1}{4} \frac{\mu C_m}{W/L} V_{in2}^2 \cdot \frac{4I_{bias}}{\mu C_m \left( \frac{W}{L} \right)^2} - \frac{4I_{bias}}{\mu C_m \left( \frac{W}{L} \right)^2} 
\end{align*}
\]

(1)

The dynamic ranges of the two differential input signals pairs for which the relation between current and voltage can be considered linear, can be written:

\[
\begin{align*}
|\Delta V_{in1}| &< 2 \left[ \frac{I_{bias}}{\mu C_m \left( \frac{W}{L} \right)^2} \right] ;
|\Delta V_{in2}| &< 2 \left[ \frac{I_{bias}}{\mu C_m \left( \frac{W}{L} \right)^2} \right]
\end{align*}
\]

(2)

The dynamic range of the proposed VGA will be studied in section III.

If the relations (2) are fulfilled, the equations (1) become:

\[
\begin{align*}
I_1 &= \frac{I_{bias}}{2} + \frac{\sqrt{2}}{4} \frac{\mu C_m}{W/L} \cdot \frac{4I_{bias}}{\mu C_m \left( \frac{W}{L} \right)^2} - \frac{4I_{bias}}{\mu C_m \left( \frac{W}{L} \right)^2} \\
I_2 &= \frac{I_{bias}}{2} - \frac{\sqrt{2}}{4} \frac{\mu C_m}{W/L} \cdot \frac{4I_{bias}}{\mu C_m \left( \frac{W}{L} \right)^2} - \frac{4I_{bias}}{\mu C_m \left( \frac{W}{L} \right)^2} 
\end{align*}
\]

(3)

The two differential output currents, noted \( i_{35} \) and \( i_{46} \) in Fig. 2 can be expressed as:

\[
\begin{align*}
i_{35} &= \frac{I_{bias}}{2} + \sqrt{2} \frac{\mu C_m \left( \frac{W}{L} \right)}{W/L} \cdot \frac{4I_{bias}}{\mu C_m \left( \frac{W}{L} \right)^2} - \frac{4I_{bias}}{\mu C_m \left( \frac{W}{L} \right)^2} \\
i_{46} &= \frac{I_{bias}}{2} - \sqrt{2} \frac{\mu C_m \left( \frac{W}{L} \right)}{W/L} \cdot \frac{4I_{bias}}{\mu C_m \left( \frac{W}{L} \right)^2} - \frac{4I_{bias}}{\mu C_m \left( \frac{W}{L} \right)^2} 
\end{align*}
\]

(4)

The two differential output currents of the VGA circuit can be written:

\[
\begin{align*}
i_{35}^* &= i_{35} - i_{46} = \frac{\sqrt{2}}{4} \frac{\mu C_m \left( \frac{W}{L} \right)}{W/L} \cdot \frac{4I_{bias}}{\mu C_m \left( \frac{W}{L} \right)^2} - \frac{4I_{bias}}{\mu C_m \left( \frac{W}{L} \right)^2} \\
i_{46}^- &= i_{46} - i_{35} = -\frac{\sqrt{2}}{4} \frac{\mu C_m \left( \frac{W}{L} \right)}{W/L} \cdot \frac{4I_{bias}}{\mu C_m \left( \frac{W}{L} \right)^2} - \frac{4I_{bias}}{\mu C_m \left( \frac{W}{L} \right)^2} 
\end{align*}
\]

(5)

In equations (5), \( \left( \frac{W}{L} \right) \) and \( \left( \frac{W}{L} \right) \) represent the aspect ratio of the transistors \( M_3, M_4, M_5, M_6 \) and \( M_1, M_2 \), respectively.

B. Differential Current to Voltage Converter

In Fig. 3, the electric scheme of the differential current to voltage converter is presented.

The two differential output voltages provided by the circuit shown in Fig. 3 can be written:

\[
\begin{align*}
V_{+} &= V_{CM} + V_{+}^* \\
V_{-} &= V_{CM} + V_{-}^* 
\end{align*}
\]

(6)

where \( V_{CM} = 1.5 V \)

and

\[
\begin{align*}
V_{+}^* &= i_{35}^* \cdot R_{conv} \\
V_{-}^- &= i_{46}^- \cdot R_{conv}
\end{align*}
\]

(7)

By using equations (5), the two differential output voltages signals from (8) can be written:

\[
\begin{align*}
V_{+} &= \frac{\sqrt{2}}{4} \frac{\mu C_m \left( \frac{W}{L} \right)}{W/L} \cdot \frac{4I_{bias}}{\mu C_m \left( \frac{W}{L} \right)^2} - \frac{4I_{bias}}{\mu C_m \left( \frac{W}{L} \right)^2} \\
V_{-} &= \frac{\sqrt{2}}{4} \frac{\mu C_m \left( \frac{W}{L} \right)}{W/L} \cdot \frac{4I_{bias}}{\mu C_m \left( \frac{W}{L} \right)^2} - \frac{4I_{bias}}{\mu C_m \left( \frac{W}{L} \right)^2}
\end{align*}
\]

(9)

C. Peak Detector Circuit

In Fig. 4, the electric schemes of both peak detectors circuits are shown.

Using the peak detectors from Fig. 4, the envelopes of the two differential signals \( V_{+}^* \) and \( V_{-}^- \) are obtained. These two envelopes are noted \( V_{peak_p} \) and \( V_{peak_n} \) in Fig. 1. To obtain the control voltage of AGC, these signals are low-pass filtered, by using simple RC filters. In this way the \( V_{control}^+ \) and \( V_{control}^- \) low frequency signals are obtained. Finally, the differential low frequency control voltage (\( V_{control} \) of the VGA circuit is obtained by summing and inverting of the \( V_{control}^+ \) and \( V_{control}^- \) low frequency signals.

Figure 3. Differential current to voltage converter

Figure 4. Peak detectors electric schemes:

a) for positive alternation; b) for negative alternation
D. Inverter Summing Amplifier

The electric scheme of the inverter summing amplifier is shown in Fig. 1. This circuit is built by using $U_{inv}$ operational amplifier and $R_1, R_2, R_3$ resistors from Fig. 1.

The output control voltage provided by the inverter summing amplifier presented in Fig. 1 can be written:

$$V_{out} = V_{CM} + V_{set} - \frac{R_3}{R_1} V_{out} - \frac{R_1}{R_2} V_{set}$$

(10)

where

$$R_1 = R_2 = R_3 = 10k\Omega$$

(11)

So, the control voltage of the second input of Gilbert cell can be written:

$$\Delta V_{in} = V_{out} - V_{CM}$$

(12)

For the ideal operation of the AGC loop, the magnitude of $V_0$ and $V_{set}$ differential signals are equal to $V_{set}$ signal which is referred to $V_{CM}$ dc level. Thus, the desired magnitude of the differential signals provided by the AGC loop can be prescribed by $V_{set}$ signal.

So, for the ideal operation of the proposed AGC loop, one should have:

$$V_{out} = 0$$

(13)

By using equations (11) and (13), the relation (10) becomes:

$$V_{out} = V_{CM} + V_{set}$$

(14)

and (12) can be expressed as:

$$\Delta V_{in} = V_{out} - V_{CM} = V_{set}$$

(15)

Thus, the proposed AGC loop provides two differential output voltages having the magnitude equal to $V_{set}$ signal.

For better performances of the proposed AGC, the dynamic range of VGA has to be as higher as possible. In order to increase the dynamic range of the VGA, the differential pair formed by the transistors $M_1$ and $M_2$ is degenerated with the $R_0$ resistor shown in Fig. 2. In this case, the differential input voltage signal $V_{in2}$ is copied over the series impedance of the two nonlinear transconductances $g_m$ and the linear degeneration resistor $R_0$ resulting in a differential signal current $i_0$ given by [6]:

$$i_0 = V_{in2} / [R_0 + 2/g_m]$$

(19)

According to equation (19) results that the gain of the proposed VGA decreases when the series resistor $R_0$ is increased. Thus, for better performances, a trade off between dynamic range and gain has to be considered in the VGA designing.

In Fig. 5.b) the dc characteristic of proposed VGA is plotted for different values of $R_0$ ($25\Omega - 250\Omega$), when control voltage is $V_{in2}=50mV$. For low values of the $R_0$ resistor, the gain of the VGA is significantly increased. But, for a bigger gain of the VGA, the closed-loop AGC operation can become instable. On the other hand, for high values of the $R_0$ resistor, the dynamic range of the VGA is increased. In our design the value of the $R_0$ resistor ($R_0 = 25\Omega$) has been chosen taken into account the observations above.

In Fig. 6 the close-loop AGC operation is illustrated, when a sinusoidal 100mVpp, 100MHz input signal modulated with $m = 0.5$ by a low-frequency of 1MHz noise is applied.

III. SIMULATIONS RESULTS

First, the dynamic range of the VGA, implemented with the Gilbert cell shown in Fig. 2 is analyzed.

In Fig. 5.a) the dc characteristic of proposed VGA is plotted for different values of $V_{in2}$ (10mV-100mV). It is obvious from Fig. 5.a) that the transconductance of Gilbert cell depends on the value of the control voltage $V_{in2}$ as equation (17) shows.

$$G_m = \frac{\sqrt{2}}{2} \Delta V_{in2} \cdot \mu C_{ox} \cdot \sqrt{\left(\frac{W}{L}\right) \cdot \left(\frac{W}{L}\right)}$$

(17)

represents the transconductance of the Gilbert cell, used as VGA, if relations (2) are fulfilled and $R_{conv}$ is the conversion resistor of the circuit shown in Fig. 3.

By using (17) in (16), the gain of the AGC loop forward path becomes:

$$A_k = G_m \cdot R_{conv} \cdot \frac{\sqrt{2}}{2} \Delta V_{in2} R_{conv} \cdot \mu C_{ax} \cdot \sqrt{\left(\frac{W}{L}\right) \cdot \left(\frac{W}{L}\right)}$$

(18)
The magnitude of the AGC differential output signals is still constant (≈200mVpp), like the outputs shown in Fig. 6. In Fig. 7 the operation of the proposed AGC is illustrated for an input signal with a frequency of 100MHz and magnitude variable in a 15mV – 100mV range. The transient regime shown detailed in Fig. 7 is due test signal which has a very small rise/fall time (50ps) for each step. According to simulations results shown in Fig. 7, the differential output signal is kept constant at ≈200mVpp. The frequency operation of the proposed AGC depends by time constant of peak detector (controlled by the discharging current) and time constants of the low-pass filters.

The main limitations of the proposed AGC are represented by the dynamic ranges of peak detector and Gilbert cell. The minimum value of AGC dynamic range is given by peak detector used, which cannot operate properly with magnitude values less than 15mV. On the other hand, the maximum magnitude value is limited by the nonlinear characteristic of Gilbert cell for value bigger than 100mV. According to these observations and simulations results, the dynamic range of the proposed AGC input signal, for which the output signal varies only with 3dB, is about 15mV – 100mV, which means 17dB.

The simulations confirm that the distortions introduced by the proposed circuit can be neglected, the differential output signal having the total harmonic distortion, \( THD < 1\% \).

It is important to note that the proposed architecture operates differentially, providing an automatic gain control amplifier for both alternations of the input signal. Thus, the control voltage of the PGA has information from both alternations of the input signal and the differential output signal magnitude is kept constant more efficiently than for other AGC architecture presented in literature.

### IV. CONCLUSIONS

In this paper a new differential CMOS automatic gain control amplifier has been presented.

The proposed architecture uses a differential variable gain amplifier implemented with a Gilbert cell and provides an automatic gain control amplifier for both alternations of the input signal. Thus, the control voltage of the PGA is given by both alternations of the input signal and the output signal magnitude is kept constant more efficiently than for other AGC architecture.

The proposed architecture yields a constant differential output magnitude of 200mVpp for an input signal having almost 20 dB dynamic range.

The simulations made in a 0.13 \( \mu \)m CMOS technology confirm the theoretical results.

### REFERENCES


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**Figure 6.** AGC waveforms for \( V_{in}=50\text{mV} \): a) input signal, \( V_{in} \); b) differential output signal (200mVpp); c) output signal positive alternation (100mVpp) and positive alternation control voltage \( V_{ctrl+} \); d) output signal negative alternation (100mVpp) and negative alternation control voltage \( V_{ctrl-} \).

**Figure 7.** AGC waveforms for an input signal with variable magnitude in a \( V_{in} = 15\text{mV} – 100\text{mV} \) range: a) variable input signal and control voltage; b) control voltage; c) differential output signal (≈200mVpp).