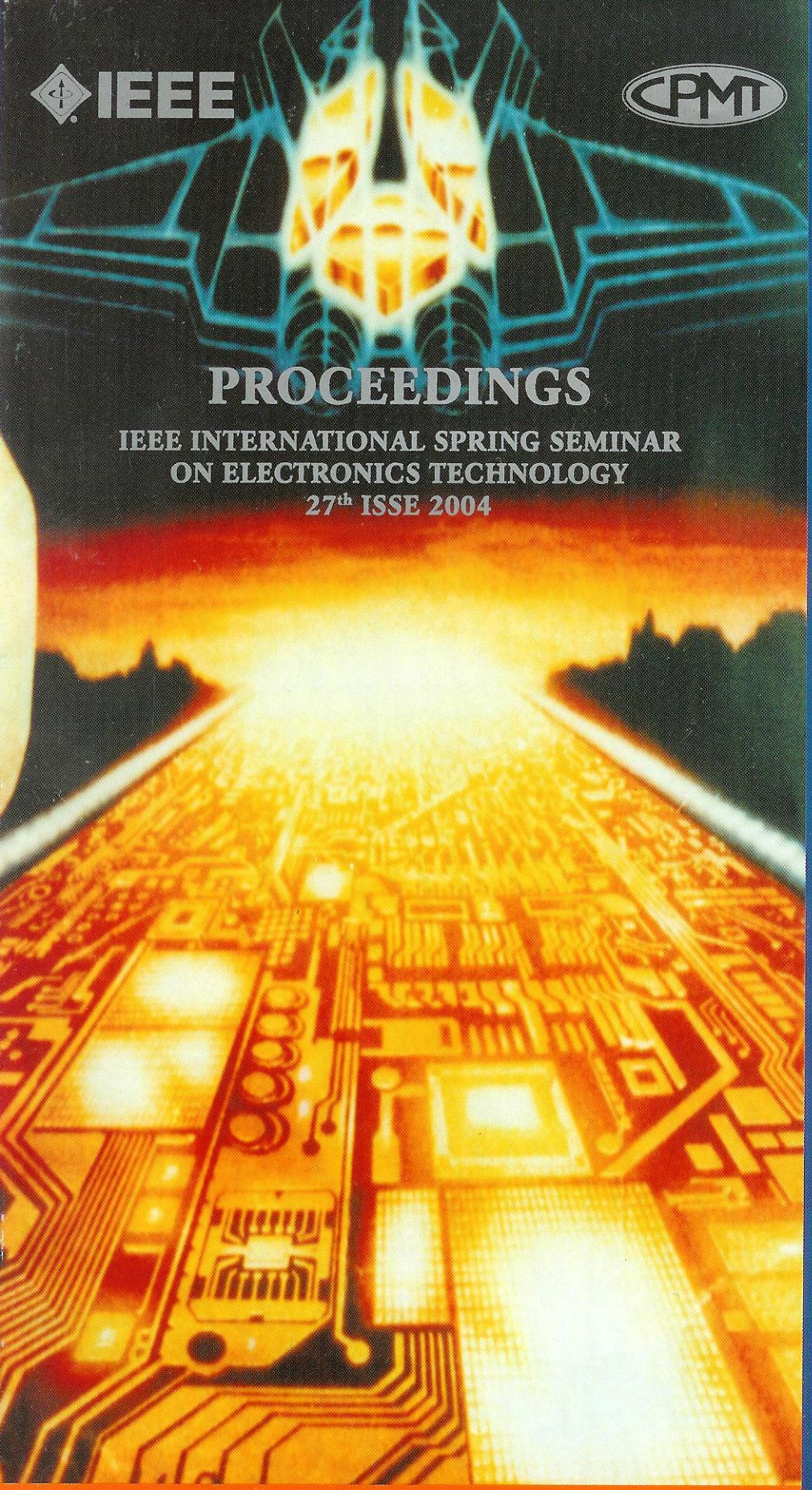

PROCEEDINGS

IEEE INTERNATIONAL SPRING SEMINAR ON ELECTRONICS TECHNOLOGY 27th ISSE 2004

Sofia, Bulgaria, May 13–16, 2004
IEEE Catalog Number 04EX830
ISBN 0-7803-8422-9
Library of Congress Number 2004102578

ANNUAL SCHOOL. LECTURES

VOLUME 24

27th International Spring Seminar on Electronics Technology ISSE 2004

Meeting the Challenges of Electronics Technology Progress

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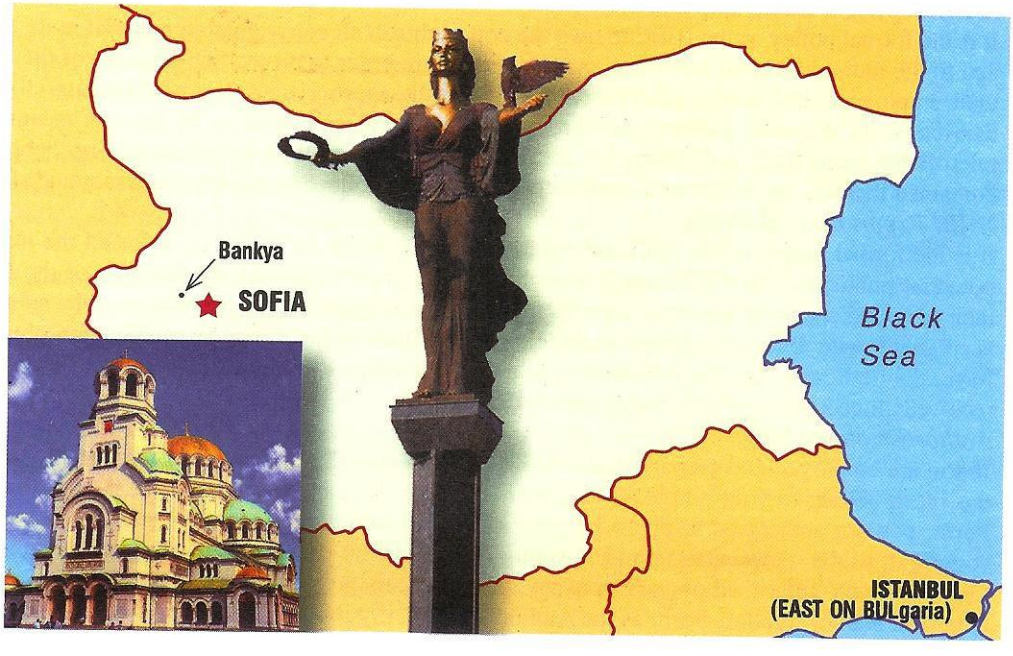

Technical University of Sofia
Department of Semiconductor- and Hybrid Technologies

13-16 May 2004
Bankya, Bulgaria

Some Aspects on Modeling and Characterization of Deep Submicrometer CMOS Gates Driving Lossless Transmission Lines

DANUT BURDIA, RADU-GABRIEL BOZOMITU, CIPRIAN-ROMEO COMSA
Faculty of Electronics and Telecommunications, "Gh. Asachi" Technical University,
Carol I, No.11 Av., 700506, Iaşi, Romania
e-mail: burdia@etc.tuiasi.ro , bozomitu@etc.tuiasi.ro

Abstract

The transient behavior of a CMOS gate driving a inductive – capacitive (lossless) transmission line is investigated in this paper. The case of input signal transition time smaller than twice the transmission line propagation delay is considered. Closed-form expressions for the output voltage and short-circuit power are derived. Also, a formula for calculating the transistor widths for the matched condition is obtained. The *n*th power law MOSFET model for short-channel devices is used. The final results are in very good agreement with SPICE simulations.
Keywords: CMOS gates, transmission line and short-circuit power.

Introduction

Currently, due to the continually scaling of CMOS technology and increasing chip size, the role of interconnect in determining circuit performance is growing in importance [1]. Interconnect modeling as a simple lumped capacitance was intensively used in the performance analysis of the VLSI circuits [2], [3].

However, the inductance is becoming more important with decreasing signal transition times and longer wire lengths [4], [5]. Therefore, more accurate RLC transmission lines models are necessary in the analysis of actual VLSI circuits. The RC and LC models can be seen as limiting cases of the RLC transmission lines models. These cases are well represented in the literature [6], [7]. The LC model approximates the low-loss lines encountered in multichip modules (MCMs) and printed circuit boards (PCBs). Although an on-chip interconnect has a non-negligible resistance, the LC analysis provides an upper limit for analyzing inductive effects in VLSI circuits.

The aim of this paper is to investigate the transient behavior of a short-channel CMOS gate driving a inductive – capacitive transmission line. The analysis is made for the case of input signal transition time less than twice of the transmission line propagation delay. Firstly, a closed-form expression for the output voltage of a CMOS inverter driving an open circuit transmission line is derived. Then, the capacitive approximation of the transmission line is analyzed, followed by the matching condition investigation, where a formula for calculating the transistor widths is obtained. Finally, the short-circuit power is analyzed and a close-form expression is derived.

Output voltage evaluation

In the following analysis consider the equivalent circuit of a CMOS inverter driving a lossless transmission line shown in Fig. 1. The output voltage derivation is for a falling input ramp

$$V_{in} = \begin{cases} V_{DD} - (V_{DD}/\tau)\cdot t & 0 \le t \le \tau \\ 0 & t > \tau \end{cases} \quad (1)$$

where τ is the input transition time. The analysis for a rising input ramp is symmetrical.

Noting T_D the transmission delay of the line, in the time interval $0 < t < 2T_D$, the transmission line can be replaced by its characteristic impedance $Z_0 = \sqrt{L_t / C_t}$, where L_t and C_t are the total inductance and capaci–tance of the line, respectively.

The *n*th power law MOS model [8] which is assumed for the transistor currents is more accurate in the linear region and in determining the drain-to-source saturation voltage as compared to the α–power law model [9], avoiding any discontinuity between the linear and saturation regions. Thus, in the saturation region ($V_{DS} \ge V_{Dsat}$), the drain current is

$$I_D = I_{Dsat} = (W/L)B\left(V_{GS} - V_T\right)^n (1 + \lambda V_{DS}) \quad (2)$$

and in the linear region ($V_{DS} \le V_{Dsat}$), the current is

$$I_D = I_{Dsat}\left(2 - \frac{V_{DS}}{V_{Dsat}}\right)\frac{V_{DS}}{V_{Dsat}} \quad (3)$$

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where $V_{Dsat} = K(V_{GS} - V_T)^m$. In these model equations, W and L are the geometric width and length, respectively, of the transistor channel, and V_T is the threshold voltage. n, m, B, K and λ are constants which describe the short-channel effects in an empirical manner. For instance, the parameter n models the carriers' velocity saturation effect taking values between 1 (for ultra-deep submicrometer devices) and 2 (for long channel devices). A comparison between the nth power law model and α–power law model is shown in Fig. 2.

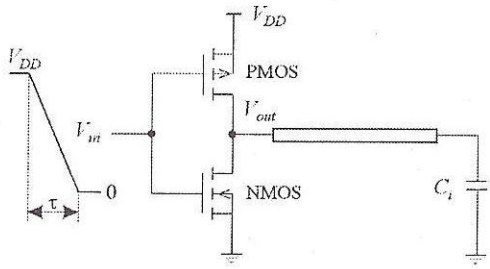

Fig. 1. CMOS inverter driving a lossless transmission line

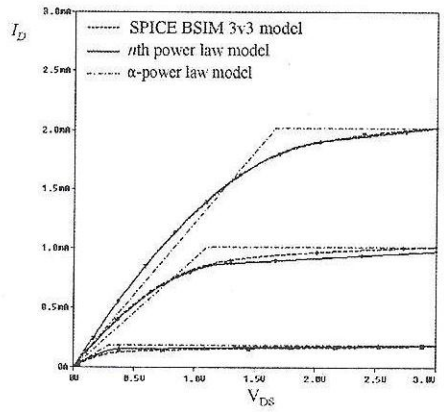

Fig. 2. Comparison between the nth power law MOS model, α-power law model and SPICE BSIM 3v3 model

For the equivalent circuit from Fig. 1, initially, the output voltage is 0. Ignoring the effect of the NMOS transistor for a falling input, after the time point $t = (V_{Tp}/V_{DD})\tau$, the PMOS transistor enters in conduction in saturation region and, consequently, the output voltage is given by the product of PMOS current and characteristic impedance of the transmission line:

$$V_{out} = Z_0 I_{psat} \tag{4}$$

Due to the fact that I_{psat} depends on both V_{in} and V_{out}, the expression for the beginning part $V_0(t)$ of the output voltage which results from (4) is

$$V_0(t) = \frac{\frac{W_p}{L_p} B_p \left(V_{DD} - V_{in} - \left|V_{Tp}\right|\right)^{n_p} (1 + \lambda_p V_{DD}) Z_0}{1 + \lambda_p \frac{W_p}{L_p} B_p \left(V_{DD} - V_{in} - \left|V_{Tp}\right|\right)^{n_p} \cdot Z_0} \tag{5}$$

At time $t = \tau$ when the input voltage reaches its final value of zero volts, the initial output voltage waveform reaches a maximum value V_1 given by

$$V_1 = \frac{I_{ps_1}(1 + \lambda_p V_{DD}) Z_0}{1 + \lambda_p I_{ps_1} Z_0} \tag{6}$$

where $I_{ps_1} = (W_p / L_p) B_p \left(V_{DD} - \left|V_{Tp}\right|\right)^{n_p}$. This initial output voltage signal, shown in Fig. 3, propagates across the line and reaches the load at time T_D.

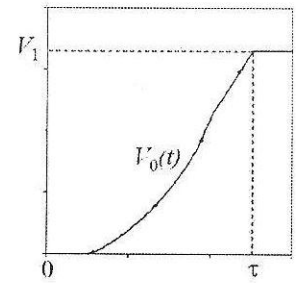

Fig. 3. The initial output voltage waveform generated by CMOS inverter during the falling input transition

Assuming the load is open or is a small capacitor, the signal reaches a steady-state value of $2V_1$ due to the reflection. The time required to reach this value depends on the time constant $Z_0 C_L$. Typically, this time constant is in order of a few picoseconds and is sufficiently small to neglect the effects of the load capacitance [5]. In the time interval $T_D < t < 2T_D$, the reflected voltage wave with the magnitude V_1 propagates back toward the CMOS inverter. At time $2T_D$, this voltage wave is reflected again by the PMOS transistor being initiated a new voltage wave with the magnitude V_2. Thus, after the time $2T_D$ the output voltage of the CMOS inverter becomes $V_{out} = 2V_1 + V_2$, as can be seen in Fig. 4. The value of V_2 is given by the impedance characteristic Z_0 multiplied by the current of the PMOS transistor with the source-to-drain voltage $V_{SDp} = V_{DD} - 2V_1 - V_2$ and source-to-gate voltage $V_{SGp} = V_{DD}$. Assuming that the PMOS transistor is in the saturation region the value of V_2 is

$$V_2 = \frac{I_{ps_1}\left[1 + \lambda_p (V_{DD} - 2V_1)\right] Z_0}{1 + \lambda_p I_{ps_1} Z_0} \tag{7}$$

For the period of time from $2T_D$ to $4T_D$ the cycle is repeated and a new voltage of magnitude V_3 is initiated at time $4T_D$. As long as the PMOS transistor is still in saturation, each new voltage wave which is initiated has a magnitude V_k calculated similar as V_2 replacing in (7) the voltage V_1 by the sum $V_1 + V_2 + \ldots + V_{k-1}$. If at the times $t = 2(k-1)T_D$ the condition $V_{DD} - 2\sum_{i=1}^{k-1} V_i - V_k \le K_p\left(V_{DD} - |V_{Tp}|\right)^{m_p}$ is satisfied, then the PMOS transistor is in its linear region and the magnitude V_k is obtained from the nonlinear equation

$$V_k = Z_0 I_{plin}(V_k) \tag{8}$$

Neglecting the channel length modulation effect in the linear region and linearizing the equation (8) around the value of zero, the resulting solution is

$$V_k = \frac{I_{ps_1}(2 - P_{k-1})P_{k-1}}{1 + \frac{4I_{ps_1}}{V_{dsp_1}}(1 - P_{k-1})} \tag{9}$$

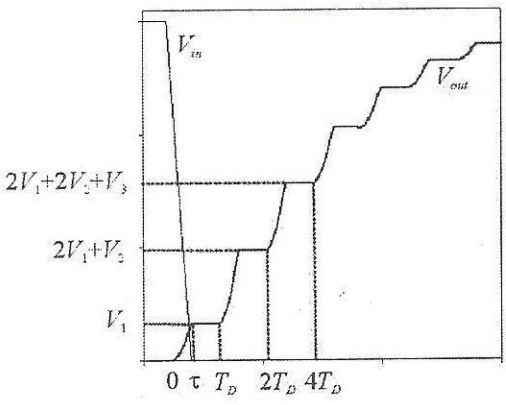

Fig. 4. Voltage waveform at the output of the PMOS transistor driving an open circuit transmission line

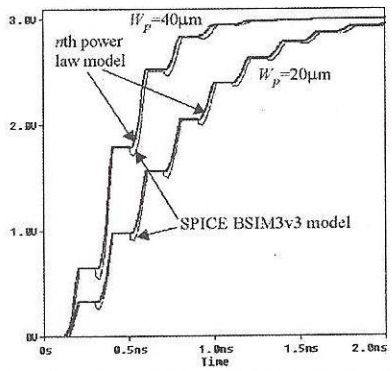

Fig. 5. Comparison between the analytical output voltage and SPICE simulations for two values of the PMOS channel width

where $P_{k-1} = \left(1/V_{dsp_1}\right)\left(V_{DD} - 2\sum_{i=1}^{k-1} V_i\right)$. The initiating process of the new wave repeats until the voltage at the output of the CMOS inverter reaches the steady state value of V_{DD}. Fig. 5 shows that the output voltage waveforms based on the analytical expressions, for two values of the PMOS channel width, are very close to the ones resulted from SPICE simulations.

Capacitive approximation of the line

The closed-form expressions of the output voltage are obtained in the previous section using for transistor currents the *n*th power law model, which describes in an empirical manner both the carriers velocity saturation effect and the channel length modulation effect, that are important for deep submicrometer technologies.

As long as the PMOS transistor is in its saturated region and the channel length modulation effect is neglected (λ_p is set to zero), its drain-to-source current has a constant value of I_{ps_1}.

After the falling voltage ramp is applied to the input of the CMOS inverter driving the transmission line, the initial output voltage wave $V_0(t)$ that propagates across the transmission line has the magnitude $V_1 = I_{ps_1} Z_0$. At the time $2T_D$, when the reflected wave of magnitude V_1 reaches the output of the inverter, the new wave that is initiated has a magnitude $V_2 = V_1$ such that the output voltage reaches the value $3V_1$, and the cycle is repeated. Thus at the times $(2k\text{-}1)T_D$, where k=1,2,...,I, the output voltage has constant values given by

$$V_{out} = (2k-1)V_1 = (2k-1)I_{ps_1} Z_0 \tag{10}$$

The horizontal parts of the output voltage have these values as long as the PMOS transistor is in the saturated region.

If the transmission line is replaced by a capacitor C_{eq}, the output voltage is

$$V_{out} = \left(1/C_{eq}\right) I_{ps_1} t \tag{11}$$

Sampling V_{out} at times $(2k\text{-}1)T_D$, the resulting values for V_{out} are given by

$$V_{out} = (2k-1)T_D I_{ps_1}\left(1/C_{eq}\right) \tag{12}$$

On the other hand, since $T_D = \sqrt{L_t C_t}$ and $Z_0 = \sqrt{L_t / C_t}$ [10], the ratio T_D/Z_0 is equal to C_t. If C_{eq} from (12) is replaced by T_D/Z_0, the expression for V_{out} becomes

$$V_{out} = (2k-1) I_{ps_1} Z_0 \qquad (13)$$

that is exactly the same as (10). Thus, the output voltage of a CMOS gate driving a capacitor $C_{eq}=C_t$ intersects the output voltage of the CMOS gate driving the transmission line at times $(2k\text{-}1)T_D$.

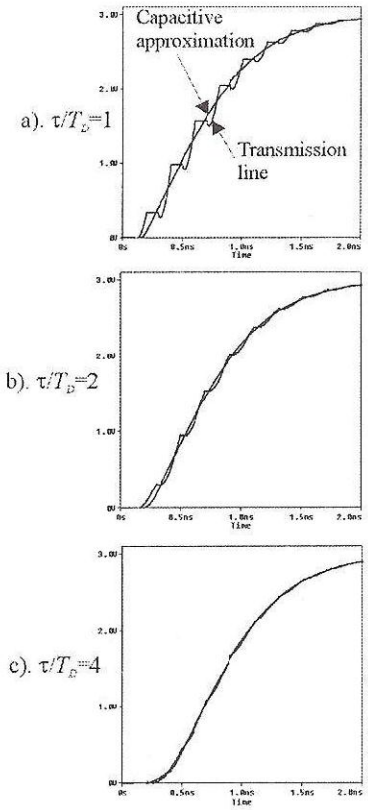

Fig. 6. Input transition time effect on the capacitive approximation of the transmission line for three values of the ratio τ/T_D.

This result is obtained neglecting the channel length modulation effect of the driving transistor to simplify the demonstration, but its validity is maintained for any complex model of the transistor, both the saturated region and the linear region, as can be seen in Fig. 6.a.

Fig. 6 shows the results from SPICE simulation based on BSIM3v3 model of a $0.25\mu m$ CMOS technology for different input transition times. As the transition time (τ) of the voltage signal at the input of the inverter increases, the transition time between the horizontal parts of the output voltage increases while the intersection points determined by the capacitance approximation remain the same. Thus, while the input transition time increases with respect to T_D, the horizontal points of output voltage become shorter and the capacitive approximation more accurately matches the transmission line, as shown in Fig. 6.b. For $\tau > 2T_D$, the horizontal portions of the response are no longer does no longer exist and the two responses coincide. Therefore, when the input transition time of the CMOS gate is greater than twice the transmission line delay, a lossless transmission line behaves as a single lumped capacitor equal to the input capacitance of the line.

Due to the fact that the signal transition times are decreasing in next generation VLSI circuits while wires are becoming longer, the most important region of interest when analyzing the effects of on-chip interconnections occurs when $\tau < 2T_D$.

Matching condition

For a given lossless transmission line with the characteristic impedance Z_0 and the time delay T_D, the number of the generated voltage waves depends on the driving capability of the transistor. Thus, if the geometric width of the transistor is small, results a small magnitude V_1 of the initial voltage signal. Also, the magnitudes of the all reflected voltage at the output of the CMOS inverter are small. In this case, due to the great number of iterations in which the signals propagate across the line, the output voltage reaches its final value of V_{DD} after a long time. For greater values of the geometric width of the transistor, the magnitudes of the signal which propagate across the line become greater and, so, a smaller number of iterations are required until the output voltage reaches its final value.

If the width of the transistor is adjusted to a value so the magnitude V_1 of the initial voltage wave that is launched to the transmission line is $V_{DD}/2$, then at time $2T_D$ when the reflected wave reaches the transistor, the output voltage becomes V_{DD}.

Consequently, the drain-to-source voltage of the PMOS transistor becomes zero volts and the transistor no longer conducts any current. Thus, there is no any reflection and the output voltage reaches its final value in a single iteration. In this case, the CMOS inverter and the transmission line are said to be matched.

The width of the PMOS transistor that satisfies the matching condition can be determined from

$$I_p\left[V_{SG_p} = V_{DD}, V_{SD_p} = V_{DD}/2\right] = \frac{V_{DD}}{2Z_0} \qquad (14)$$

where $I_p\left[V_{SG_p}=V_{DD}, V_{SD_p}=V_{DD}/2\right]$ is the PMOS transistor current when the source-to-gate voltage is V_{DD} and the source-to-drain is $V_{DD}/2$. Due to early saturation phenomena of deep submicrometer devices [9], equation (14) is resolved considering the nth power law model of the transistor current for saturation region. Thus, the geometric width W_{p_M} of the PMOS transistor for the matched condition is

$$W_{p_M}=\frac{V_{DD}}{2Z_0\frac{B_p}{L_p}\left(V_{DD}-\left|V_{Tp}\right|\right)^{n_p}\left(1+\lambda_p\frac{V_{DD}}{2}\right)} \quad (15)$$

The geometric width W_{n_M} of the NMOS transistor for the matched case is obtained in a similar manner. The CMOS inverter is full matched to a transmission line if both PMOS and NMOS transistors are matched to the line. In this case, the output impedance of the CMOS inverter is equal to the characteristic impedance of the line for both rising and falling input ramp.

The line is said to be underdriven if the widths of the transistors of the CMOS inverter driving the transmission line are smaller than the transistor widths in the matched case, such that the output impedance of the CMOS inverter is greater than the characteristic impedance of the line. If wider transistor are used, as compared to the matched widths, the output impedance of the CMOS gate is smaller than the value of Z_0 and the output response is overdriven with overshoots and undershoots.

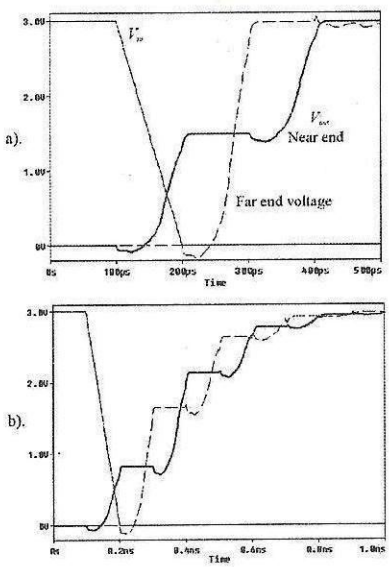

Fig. 7. SPICE simulation for a CMOS inverter driving a lossless transmission line a). matched case b). underdriven case

Fig. 7.a. shows the SPICE simulations for the matched condition that demonstrate the accuracy of the equation (15), while Fig. 7.b. illustrates an underdriven case (the channel width is half of matching width).

Short-circuit power dissipation

The power dissipated in a CMOS gate driving a transmission line consists of dynamic (or switching) power, leakage (or stand-by) power and short-circuit power components.

The dynamic power is due to the current which charges the transmission line and is the same as the dynamic power consumption of a CMOS gate driving a capacitor equal to the total capacitance of the transmission line [11].

The short-circuit power is dissipated when both the NMOS and PMOS transistors conduct at the same time, namely during the time interval when the rising (falling) input voltage is between V_{Tn} and V_{DD}-$|V_{Tp}|$, where V_{Tn} is the threshold voltage of the NMOS transistor. This power is investigated below for the case when $\tau<2T_D$. In this case, the reflections do not affect the short-circuit power because the initial output signal has reached its final value. Therefore, for the time interval 0 to τ, the transmission line appears as a resistance with a value of Z_0. Considering the case of rising input voltage $V_{in}=(V_{DD}/\tau)t$, the line is assumed to be charged to V_{DD}. The equivalent circuit used to determine the short-circuit power is shown in Fig. 8.

In order to obtain good results, the gate-to-source capacitance C_{GSp} of the PMOS transistor is taken into account. Thus, the short-circuit current I_{SC} is given by

$$I_{SC}=I_p-I_{GS} \quad (16)$$

where I_p is the source-to-drain current of the PMOS transistor and I_{SC} is the current trough capacitor C_{GSp}.

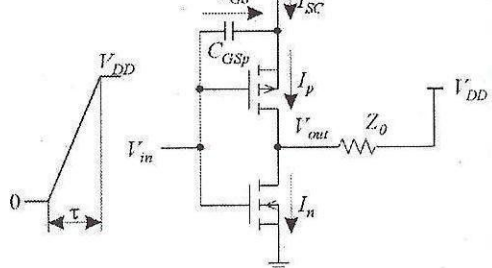

Fig. 8. The circuit used to determine the short-circuit power

During the first part of the rising input voltage, the PMOS transistor operates in the linear region and, after that, it enters in the saturation region. When the PMOS transistor operates in the linear region, the current Ip is given by

$$I_p = \frac{W_p}{L_p} B_p \left(V_{DD} - \frac{V_{DD}}{\tau} t - \left|V_{Tp}\right| \right)^{n_p} \cdot \left(2 - \frac{V_{DD} - V_{out}}{V_{DSAT_p}} \right) \left(\frac{V_{DD} - V_{out}}{V_{DSAT_p}} \right) \left[1 + \lambda_p \left(V_{DD} - V_{out} \right) \right] \quad (17)$$

where $V_{DSAT_p} = K_p \left(V_{DD} - \frac{V_{DD}}{\tau} t - \left|V_{Tp}\right| \right)^{m_p}$ and V_{out} is the output voltage of the CMOS inverter, expressed as $V_{out}=V_{DD}-V_0(t)$. Here, $V_0(t)$ is the initial voltage pulse with negative from equation (5), except the index p is replaced by n.

When the PMOS transistor is in the saturated region, the current Ip is

$$I_p = \frac{W_p}{L_p} B_p \left(V_{DD} - \frac{V_{DD}}{\tau} t - \left|V_{Tp}\right| \right)^{n_p} \cdot \left[1 + \lambda_p \left(V_{DD} - V_{out} \right) \right] \quad (18)$$

The current I_{GS} is given by

$$I_{GS} = C_{GSp} \frac{\mathrm{d}\left(V_{in} - V_{DD}\right)}{\mathrm{d}t} = C_{GSp} \frac{V_{DD}}{\tau} \quad (19)$$

Because C_{GSp} has different values in the linear and saturation regions, I_{GS} has the constant values I_{GS1} and I_{GS2} when PMOS transistor operates in the linear region and saturation region, respectively.

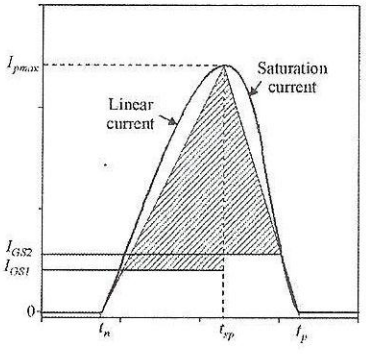

Fig. 9. Linear approximation of the drain-to-source PMOS current. Short-circuit energy is represented by dashed area.

The short-circuit energy dissipated during an input transition can be evaluated as a product between V_{DD} and the area delimited by PMOS current I_p and capacitive current I_{GS}. This area can be evaluated simpler if a linear approximation of I_p current is used, as shown in Fig. 9. In this figure $t_n = \left(V_{Tn}/V_{DD}\right)\tau$ and $t_p = \left(V_{Tp}/V_{DD}\right)\tau$ define the times when NMOS transistor starts to conduct and PMOS transistor becomes off. Time t_s corresponds the moment when PMOS transistor enters in saturation region and is a solution equating the two expressions (17) and (18) of PMOS current for linear and saturation regions, respectively. Because t_s can not be obtained analytically, it is expressed as

$$t_s = t_n + \theta\left(t_p - t_n\right) \quad (20)$$

where θ is a constant. From experiments, a good approximation for θ is 0.65.

At time t_s the PMOS current has a maximum value I_{pmax} that can be obtained evaluating any of the expressions (17) or (18) for $t=t_s$.

Based on this approximations, the short-circuit energy is the product of V_{DD} and dashed area shown in Fig. 9 and is

$$E_{SC} = \frac{V_{DD}}{2} \left[t_x \left(I_{p\max} - I_{GS1} \right) + t_y \left(I_{p\max} - I_{GS2} \right) \right] K_a \quad (21)$$

where $t_x = \frac{I_{p\max} - I_{GS1}}{\theta\left(t_p - t_n\right)}$ and $t_y = \frac{I_{p\max} - I_{GS2}}{\left(1-\theta\right)\left(t_p - t_n\right)}$ and K_a is a correction factor used to compensate the underestimation of the area.

Table 1 presents the results of the short-circuit energy dissipation evaluated by analytical expression compared to SPICE simulation. As can be seen, the error is smaller for greater values of short-circuit energy. For smaller channel widths, the errors are greater than 20%, but the energy values are insignificant.

TABLE 1. SPICE and analytical results of short-circuit energy for different values of the width to matched width ratio (W/W_M)

W/W_M	SPICE [fJ]	Analytical [fJ]	Error [%]
1.2	481.35	472.67	1.73
1	332.70	324.70	2.20
0.75	187.50	181.55	3.17
0.5	53	48.22	9.02
0.3	7	5.38	23.14
0.2	0	0	-

Conclusions

The switching behavior of a short-channel CMOS gate driving a lossless transmission line was investigated. The case of input signal transition time less than twice of the transmission line propagation delay was considered. This is the case when the transmission line effects are significant. Based on the *n*th power law MOSFET model, a closed-form expression for the output voltage of a CMOS inverter driving a transmission line ended by an open circuit (or small capacitor) is derived. Also, it has been shown that the line can be approximated by a lumped capacitor if the input transition time is greater than twice the propagation delay of the line. A formula for calculating the transistor widths for the matched condition is obtained. Finally, a close-form short-circuit power expression is derived.

followed by the matching condition investigation, where a formula for calculating the transistor widths is obtained. Finally, the short-circuit power is analyzed and a close-form expression is derived.

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